In the Claims:

Please amend the Claims as follows:

1. (Currently Amended) A method of processing loop instructions using a data processing device having a central processing unit (CPU) and a coprocessor, wherein the CPU fetches and predecodes instructions retrieved from program memory and determines whether the instructions are CPU-type or coprocessor-type, comprising the steps of:

decoding the coprocessor-type instructions by the coprocessor and if a loop operation is decoded, retrieving from the program memory the instructions within the loop;

storing the retrieved instructions within the loop in a loop buffer;

executing at least one coprocessor-type instruction from the loop buffer by the coprocessor, and forwarding any CPU-type instructions from the loop buffer to the CPU for execution; and

inhibiting instruction fetch from the program memory while instructions within the loop are executed in a subsequent iteration of the loop.

2. (Original) The method of Claim 1, further including the step of accessing the instructions within the loop from the loop buffer in a subsequent iteration of the loop.

3. (Previously Presented) The method of Claim 1, further including

determining a backward branch distance for use by the CPU to control branching to and from the loop.

4. (Original) The method of Claim 1 further including the steps of:

determining from the loop instruction a number of iterations of the loop operation;

decrementing by the coprocessor the number of iterations upon completion of each loop; and

signaling to the CPU the completion of the loop operation when reaching the end of the number of iterations.

5. (Original) The method of Claim 1, wherein said storing step includes storing 'n' loop instructions in 'm' registers of the loop buffer and addressing the 'm' registers by $\log_2 m$ least significant bits (LSBs) of a program counter which is also used for addressing the program memory, wherein n or m is any natural number and n is less than or equal to m.

6. (Original) The method of Claim 5, further including the steps of accessing the instructions stored in the loop buffer through a multiplexer and controlling the multiplexer output by the $\log_2 m$ LSBs of the program counter.

7. (Previously Presented) The method of Claim 5, wherein a first instruction

within the loop is stored in one of the m registers addressed by the LSBs of the program counter.

8. (Original) The method of Claim 1, further including the steps of signaling the presence or absence of an active loop instruction by a loop buffer flag in each of the 'm' registers in the loop buffer, the presence of an active instruction in a register is indicated by a preassigned signal in the loop buffer flag.

9. (Original) The method of Claim 8, further including the step of accessing each flag in the loop buffer by $\log_2 m$ least significant bits of a program counter used for addressing the program memory.

10. (Original) The method of Claim 8, further including the step of multiplexing an instruction from the loop buffer and the program memory, the multiplexing is dependent upon a presence of an active instruction signal from a loop buffer flag.

11. (Original) The method of Claim 8, wherein said step of inhibiting instruction fetch from the program memory includes sending an inhibit signal to the program memory when the preassigned signal in the loop buffer flag is read and indicates the presence of an active loop instruction.

12. (Original) The method of Claim 11, wherein the preassigned signal in

each of said loop buffers is selectively alterable by the CPU independent of the presence or absence of an active instruction in corresponding registers.

13. (Original) The method of Claim 8, further including the step of clearing the loop buffer flag when the loop operation is completed.

14. (Currently Amended) A data processing device comprising:

a central processing unit (CPU) for fetching instructions from a program memory, predecoding the instructions and sending a signal (CCLK) to a coprocessor if a ~~coprocessor~~ coprocessor-type instruction is decoded;

a coprocessor for decoding the coprocessor-type instructions upon receipt of the signal (CCLK); and

a loop buffer for receiving from the program memory instructions within a loop and storing the instructions within the loop when the coprocessor decodes a loop operation from the coprocessor-type instructions, wherein the instructions within the loop are retrieved from the loop buffer for execution in a subsequent iteration of the loop, and wherein the loop buffer instructions of coprocessor-type are executed by the coprocessor and the loop buffer instructions of CPU-type are forwarded to the CPU for execution.

15. (Original) The device of Claim 14, wherein a disable signal is sent to the program memory for inhibiting access of the program memory while the instructions

within the loop are retrieved from the loop buffer.

16. (Original) The device of Claim 14, wherein the loop buffer includes 'm' registers, each having a corresponding loop buffer flag for indicating whether the corresponding register is filled with an instruction.

17. (Original) The device of Claim 16, wherein the loop buffer flags are accessed by $\log_2 m$ least significant bits of a program counter used for addressing the program memory.

18. (Original) The device of Claim 16, wherein a program memory inhibit signal is generated based on a signal read from the loop buffer flag.

19. (Original) The device of Claim 14, wherein the loop buffer includes 'm' registers and the registers are addressed by $\log_2 m$ LSBs of a program counter used for addressing the program memory.

20. (Previously Presented) The device of Claim 16, further including a multiplexer for multiplexing between the instructions retrieved from the program memory and the instructions retrieved from the loop buffer, the multiplexor being controlled by signals read from the loop buffer flags.

21. (Original) The device of Claim 14, wherein the coprocessor decodes from a loop instruction a loop block size and a number of iterations of looping, and calculates a backward branch distance for use by the CPU to control branching to and from the loop.

22. (Original) The device of Claim 21, wherein the backward branch distance is the loop block size minus one.

23. (Canceled)

24. (Currently Amended) A data processing device comprising:

a central processing unit (CPU) for fetching instructions from a program memory, predecoding the instructions and sending a signal (CCLK) to a coprocessor if a ~~coprocessor~~ coprocessor-type instruction is decoded;

a coprocessor for decoding the coprocessor-type instructions upon receipt of the signal (CCLK); and

a loop buffer for receiving from the program memory instructions within a loop and storing the instructions within the loop when the coprocessor decodes a loop operation from the coprocessor-type instructions, wherein the instructions within the loop are retrieved from the loop buffer for execution in a subsequent iteration of the loop, wherein the loop buffer instructions of coprocessor-type are executed by the coprocessor and the loop buffer instructions of CPU-type are forwarded to the CPU for

execution, and wherein a disable signal is sent to the program memory for inhibiting access of the program memory while the instructions within the loop are retrieved from the loop buffer.